IJETAE
EXPLORING RESEARCH AND INNOVATIONS

International Journal of Emerging Technology and Advanced Engineering
Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 6, Issue 9, September 2016)

Comparative Study of PMOS Field Effect Transistor and Silicon on Insulator PMOS Field Effect Transistor

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***Abstract*— Silicon on insulator (SOI) PMOS FET transistor is designed as single gate device which is three dimensional. This device offers a higher current drive per unit silicon area than conventional PMOSFETs. SOI technology is a promising good electrical performance of the devices and with high quality SOI material also improved its electrical parameters by comparing these two devices. For analyzing these devices VLSI TCAD simulator is used.**

***Keywords*— PMOSFET, Silicon on Insulator, TCAD.**

I. INTRODUCTION

The demand for faster and cheaper electronic devices has an incredible shrinking of device area and a corresponding increase in component density. This type modern technology brings with it some difficult problem as heat transfer. The thermal power is induced at many device junctions, and the heat needs to diffuse away from the components of the devices, or the devices would suffer from self heating effects, this includes degradation of reliability and electronic performance[1-2]. The first field effect transistor concept, as "Method and Apparatus for Controlling Electric Currents" about 80 years ago, which came into the modern metal oxide semiconductor field effect transistor, MOSFET [3]. The 3-terminal device as source to drain current is controlled by the gate field [2-4]. The active device was built on a thin semiconductor thickness which is deposited on an insulator [4]. The first proposed field effect transistor was indeed, a SOI device and gave the concept; unfortunately, very fast concept was too fictional to be produced by the technology. Gordon Moore in 1965 proposed as well known Moore's Law; this proposed Law explained the evolution of the transistor density in integrated circuits. And the prediction was the number of transistors per chip would quadruple every three years. So this type technological development enhances the industrial growth followed the Moore's Law for the past 40 years. Silicon technology has progressed faster year to year. The main issue is to be concentrate about silicon technology, the silicon device can be scaled down reducing the dimension of devices and increasing the circuit complexity which is consistently been achieved by aggressive of scaling the semiconductor device dimension.

Power consumption of ultra large scale integration (ULSI) circuits is very serious problems, when a silicon metal-oxide semiconductor field-effect transistor (MOSFET) that has dimension goes down into the deep submicron range. The major problem of the source-drain junction formation, which avoid short channel effect at nano-scale range device[5-6,7], to reduce this problem, a new circuit design techniques been introduced[8-9,10,11].The adoption of Silicon on Insulator substrates for the semiconductor devices such as integrated circuits has given SOI research an unprecedented impetus[12-14]. The process simplicity and other benefitted such as reduced parasitic capacitance and reduced the short channel effect is the reason to the development of silicon on insulator MOSFET. SOI–MOSFET transistor has been found to be more effective than ordinary transistor that is made of semiconductor material. The long channel SOI MOSFET's has larger current drive than bulk MOSFET's [13-14].

II. STRUCTURE OF SOI PMOSFET

The device structure has top oxide layer to insulate the gate from the channel 't_{ox1}'is 0.017µm, silicon thickness 't_{Si}' is 0.1µm, bottom oxide layer 't_{ox2}' is 0.3µm thick, and the gate and channel width is 1µm. The electrodes on the source and drain cover 0.5µm on each end of the device. The entire silicon region is covered n-type doping of $1x10^{20}cm^{-3}$, and area on either side of the channel is p-type of doping of $2x10^{17}cm^{-3}$. The interface charges on the top of the silicon are $3x10^{10}cm^{-3}$ and the interface charge on the bottom of the silicon region are $1x10^{11}cm^{-3}$, and the work function of the gate material (p-type poly silicon) is 4.17eV.The structure is shown in figure 1.

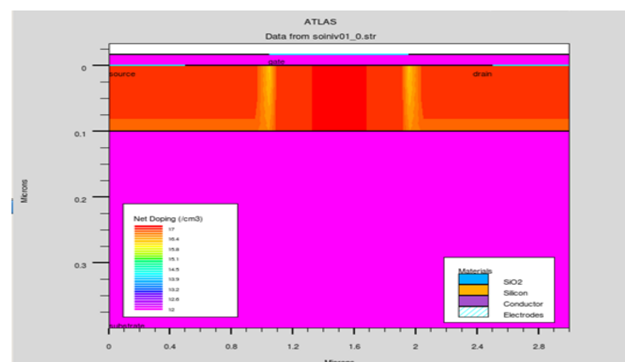

Fig. 1 Silicon on Insulator (SOI) PMOSFET structure

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III. RESULT AND DISCUSSION

I_d-V_g Characteristics of SOI PMOSFET

The figure2, shown here is the I_d-V_g characteristics; at the lower values of V_g (< 0.2V) large drain current obtained and flow linearly but it is decreases as increases the gate voltage till V_g=0.2V. Beyond the 0.2V the current is still decreases non-linearly as gate voltages increases.

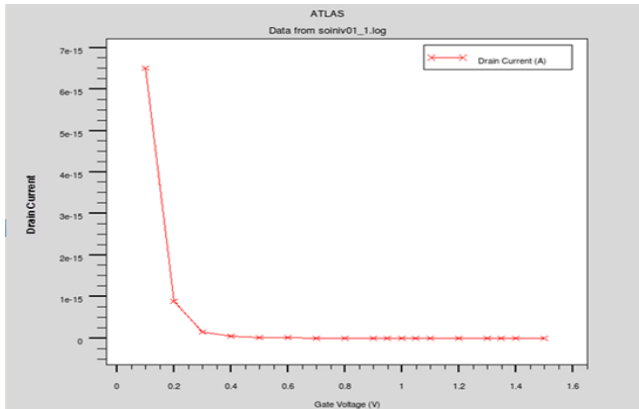

Fig.2. Transfer Curve of SOI PMOSFET

The figure3, shown is the gate voltage versus drain current of conventional PMOSFET here the figure 3 denoted as V_g of negative value is decreases the current is being reduced as shown in the figure 3. I_d initially gradually decreases when the gate voltage is increased from -3V to -1V but as V_g> -1V , the drain current will become nearly zero, where as in SOI MOSFET there is a large positive drain current flows through the device when the device is on, therefore the SOI PMOSFET devices are better for Analog devices over PMOSFET.

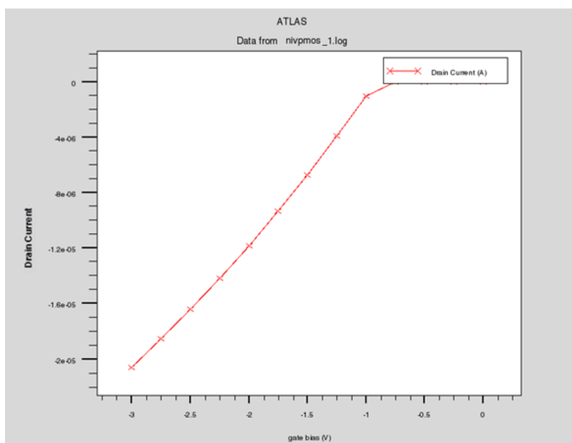

Fig.3. Gate voltage versus drain current of PMOSFET

I_d-V_d Characteristics of SOI PMOSFET

The figure4 shown as variation of I_d (drain current) due to V_d in different values when V_g as constant for the different values of drain voltages.

In this figure4 each plot represent as the ohmic (active) region, nonlinear region and the saturation region. Ohmic region-constant resistance region, if drain to source voltage is zero, the drain current also zero regarding gate to source voltage applied. In this region I_d followed linear in nature; initially, when V_g is 0V (shown by red line) drain voltage applied and increases up to -1VAgain now V_g is changed as V_g= -1.0V (shown by sky blue line) with drain voltage up to -0.5V. Similarly, V_g= -2.0V (shown by dark blue line) and drain voltage decreased as -0.42V, when the V_g is increased as -3.0V (shown by green line) V_d becomes highly proportional to decreased in voltage up to -0.34V.

Non Linear Region: I_d obtained nonlinear pattern in nature: first condition, when V_g = 0V (shown by red line) and drain voltage from -1V to -3V. Second condition, when V_g at -1.0V (shown by sky blue line) and drain voltage from -0.5V to -02.42V. Third condition, when the V_g is increased to -2.0V (shown by dark blue line) the drain voltage vary from -0.42V to -1.84V.

Saturation Region: Constant current region. In this region, the drain current differs to the other region such as in this region, even drain voltage increased but drain current did not increased by the gate to source voltage. Here, there are overlay plots for different values of gate voltages.

Cut Off Region: It is called cut off region, when the gate to source voltage is lower than V_g (th) (threshold voltage).With V_g= -4V the drain current becomes nearly zero independent to the variation of drain voltage.

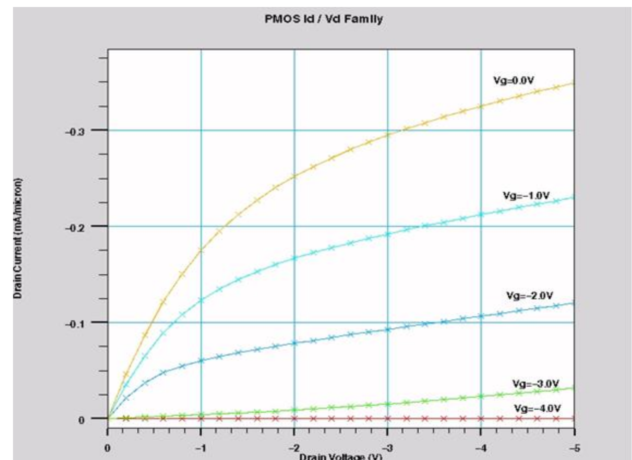

Fig.4. Drain current versus drain voltage Characteristics of SOI PMOSFET

IV. CONCLUSION

Silicon on insulator (SOI) PMOSFET transistors is evolving from the classical, planar, single-gate device into three dimensional devices. These devices offer a higher current drive per unit silicon area than conventional PMOSFETs.

SOI technology is a promising good electrical performance of the devices and high quality SOI material continues to improve it again. Thickness of SOI material influences the electrical parameter of the device, such as threshold voltage.SOI technology is a good candidate for future in VLSI technology as the quality of SOI material continues to also improve in high temperature application.

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